// VerilogA for ADC\_Ideal\_4bit\_FlashADC, VerilogA\_ClockedComparator, veriloga

`include "constants.vams"

`include "disciplines.vams"

module VerilogA\_ClockedComparator(dout,vref,vin,clk);

parameter real clk\_th=0.9;

parameter real delay = 0;

parameter real ttime = 1p;

input vin,vref,clk;

output dout;

electrical dout,vref,vin,clk;

real d\_result;

analog begin

@(cross(V(clk) - clk\_th, -1)) begin

if(V(vin) > V(vref)) begin

d\_result = 1;

end

else begin

d\_result = 0;

end

end

@(cross(V(clk) - clk\_th, +1)) begin

d\_result = 0;

end

V(dout) <+ transition(d\_result,delay,ttime);

end

endmodule